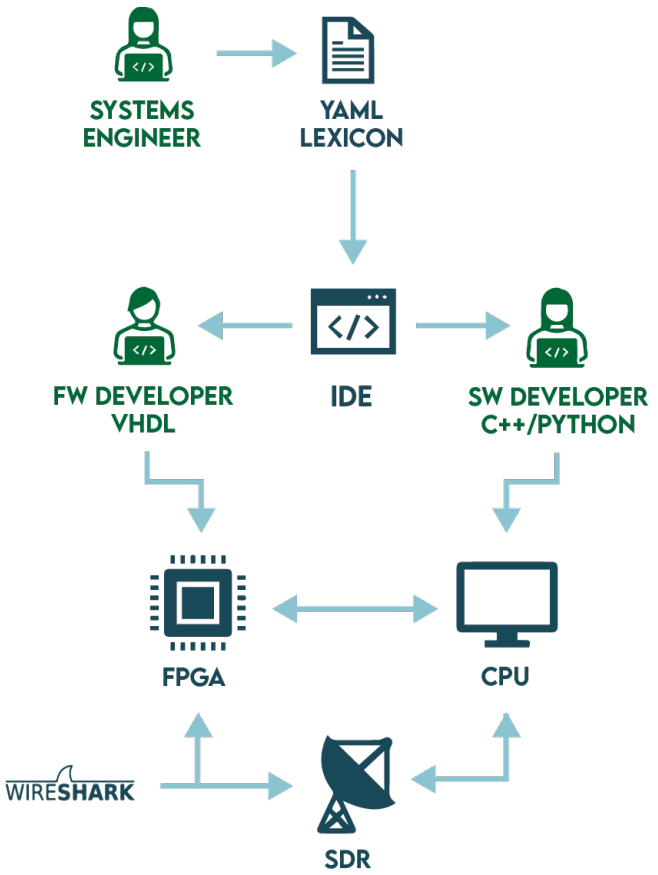
VITA 49.2

PRODUCT DETAILS

The VITA 49.2 Subsystem is Geon's extensible Intellectual Property (IP) core for ANSI/VITA 49.2-2017 compliant communications on a programmable logic device. VITA 49.2 provides standardized communications across the system while remaining agnostic of the transport backbone used (UDP/IP, PCIe, Aurora, etc). VITA 49.2 is a highly customizable standard, and Geon's advanced IP core technology is optimized to meet your project's unique requirements with minimal resource utilization.



SUPPORTED FEATURES

- VITA 49.2 Data, Context, and Command packet parsing and encapsulation
- VITA 49.2 Controllee role for the implementation of radio frontends or hardware accelerators
- VITA 49.2 Controller role to implement low-latency FPGA-based controllers
- VITA 49.2 Packet Classes to process packet definitions from multiple vendors or organizations
- Either "in-band" (on the same link as Data/Context packets) or "out-of-band" VITA 49.2 Command packet flow
- Multi-channel implementations for high-rate data using multiple VITA 49.2/UDP/IP stacks (UDP/IP core available at additional cost)
- Multi-stream implementations for low-rate data using a single VITA 49.2/UDP/IP stack and multiple stream identifiers
- Standard AXI4 interfaces: AXI4-Stream for data interfaces and AXI4-Lite for register control

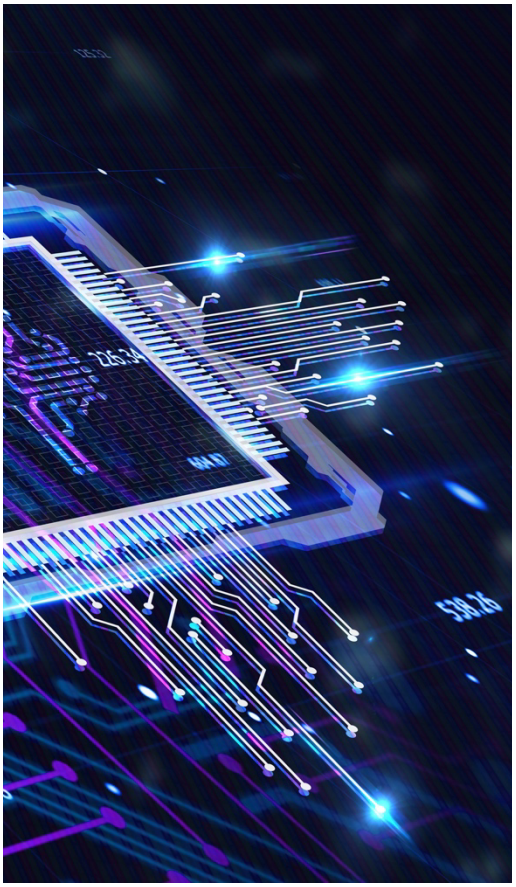
See the Product Guide for detailed port descriptions, register maps, and limitations

DELIVERY

Core is available in two delivery configurations:

- Encrypted: All source code is encrypted except for a reference testbench and all constraints files
- Source Code: All source code may be viewed and changed

Geon



INCLUDED WITH PURCHASE

1. Embedded C++ software utility for register control and Bitbake recipe to cross compile with Yocto or Petalinux
2. Host C++ packet processing software for communicating with the core over a UDP/IP network
3. Wireshark plugin for packet analysis over a UDP/IP network
4. Reference project for one of the following platforms:
   - Picozed 7030 FMC2 (Zynq-7000) with 1GbE
   - ZCU102 (Ultrascale+) with 10GbE
   - ZCU111 (Ultrascale+) with 10GbE
   - ZCU208 (Ultrascale+) with 10GbE
   - ZCU216 (Ultrascale+) with 10GbE
   - ZCU111 (Ultrascale+) with 100GbE

VITA
Open Standards, Open Markets

CONTACT US FOR A QUOTE TODAY!

LICENSING

Our site license allows the IP core to be used in an any project created within the building or campus designated as the "licensed site."

TERMS AND CONDITIONS

Geon delivers the VITA 49.2 Subsystem FPGA IP core specifically tailored to a customer's requirements. When customer requirements change and modifications to the core are required, Geon will reconfigure the core for a fee, and this fee includes updates to the latest version of Geon's codebase.

Geon will fix functional flaws in the core for 1 year after date of purchase at no cost. Support that is not related to a functional flaw or all support beyond 1 year after date of purchase can be provided at an hourly consulting rate.