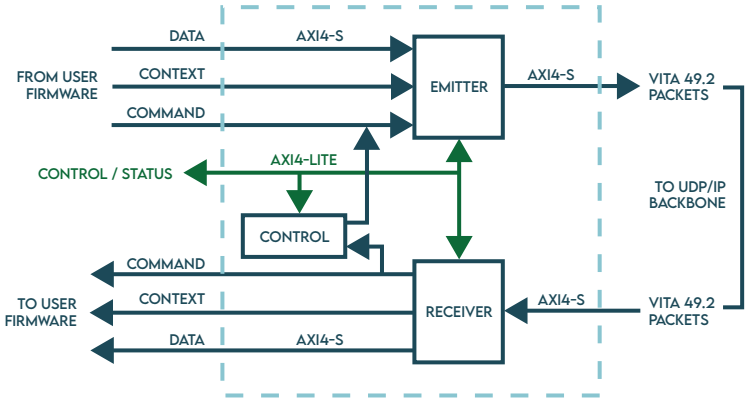
VITA 49.2

PRODUCT OVERVIEW

The VITA49.2 Subsystem is Geon Technologies' extensible Intellectual Property (IP) core for ANSI/VITA49.2-2017 compliant communications on a programmable logic device. VITA49.2 provides standardized communications across the system while remaining agnostic of the transport backbone used (UDP/IP, PCIe, Aurora, etc).

VITA49.2 is a highly customizable standard, and Geon's advanced IP core technology is optimized to meet your project's unique requirements with minimal resource utilization.

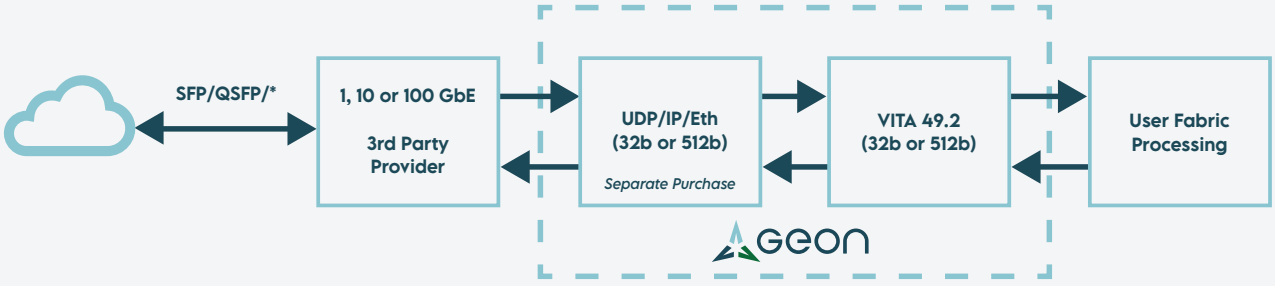
VITA 49.2 IP CORE



SUPPORTED FEATURES

- VITA49.2 Data, Context, and Command packet parsing and encapsulation
- VITA49.2 Controllee and Controller roles
- Standard AXI4 interfaces: AXI4-Stream for data interfaces and AXI4-Lite for register control
- FPGA vendor independent
- Purchase options for supporting 32 bit and 512 bit configurations for targeting 1 GbE, 10 GbE, and 100 GbE backbones
- See the Product Guides (32 bit and 512 bit) for detailed port descriptions, register maps, and limitations

TYPICAL APPLICATION



CONTACT

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PRODUCT DETAILS

CORE PART NUMBERS

geon_ip_00.00.01
32 bit (1 GbE / 10 GbE backbone)

geon_ip_00.00.11
512 bit (100 GbE backbone)

DELIVERY

The core is available in two delivery configurations:

ENCRYPTED: All source code is encrypted except for a reference testbench and all constraints files

SOURCE CODE: All source code may be viewed and changed

LICENSE

SITE-WIDE: The core may be used on all projects within the organization

ADDITIONAL SUPPORTED FEATURES

- VITA49.2 Packet Classes to process packet definitions from multiple vendors or organizations
- Either "in-band" (on the same link as Data/Context packets) or “out-of-band" VITA49.2 Command packet flow
- Multi-channel implementations for high-rate data using multiple VITA49.2/UDP/IP stacks (UDP/IP core available at an additional cost)
- Multi-stream implementations for low-rate data using a single VITA49.2/UDP/IP stack and multiple stream identifiers

INCLUDED WITH PURCHASE

- Wireshark plugin for packet analysis over a UDP/IP network
- Embedded C++ software utility for register control and Bitbake recipe to cross compile with Yocto or Petalinux
- Host C++ packet processing software for communicating with the core over a UDP/IP network
- Reference project for one of the following platforms:
  - Picozed 7030 FMC2 (Zynq-7000) with 1GbE
  - ZCU102 (UltraScale+) with 10GbE
  - ZCU111 (UltraScale+) with 10GbE
  - ZCU208 (UltraScale+) with 10GbE
  - ZCU216 (UltraScale+) with 10GbE

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