

STANDARDS-COMPLIANT FPGA COMMUNICATIONS

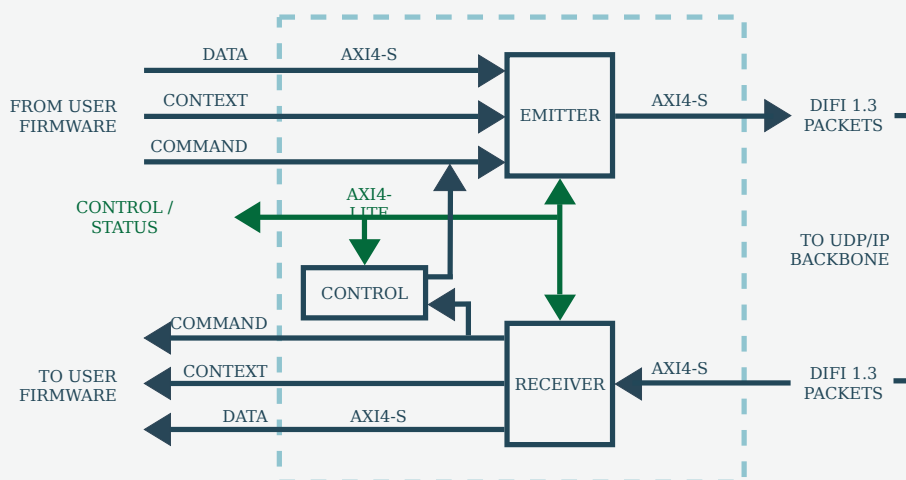
DIFI 1.3

An FPGA IP core implementing the DIFI 1.3 digital IF standard — including full link establishment between Source and Sink

KEY BENEFITS

- DIFI 1.3 (ISTO 4900) link establishment
- Source (Controller) and Sink (Controllee) roles
- In-band negotiation — no side channel
- Context validation and status reporting
- Transport agnostic (UDP/IP, PCIe, Aurora)
- Rapid AXI-based integration

DIFI 1.3 IP CORE



CORE FEATURES

LINK ESTABLISHMENT

0x0007 Query · **0x0008** Response · **0x0009** Status Report, driven by a five-state negotiation FSM in fabric.

INFORMATION CLASSES

Basic Data Plane (0x0000) plus the link-bearing classes 0x0100–0x0106 and Standalone Link Establishment (0x0101).

CONTEXT VALIDATION

14 conformance checks on every Signal Context, including per-class Timestamp Mode, with bit-accurate error codes returned to the Source.

DATA INTEGRITY

Signal Data timestamped during a Context Error is disregarded in hardware, scoped to the link's own Information Class.

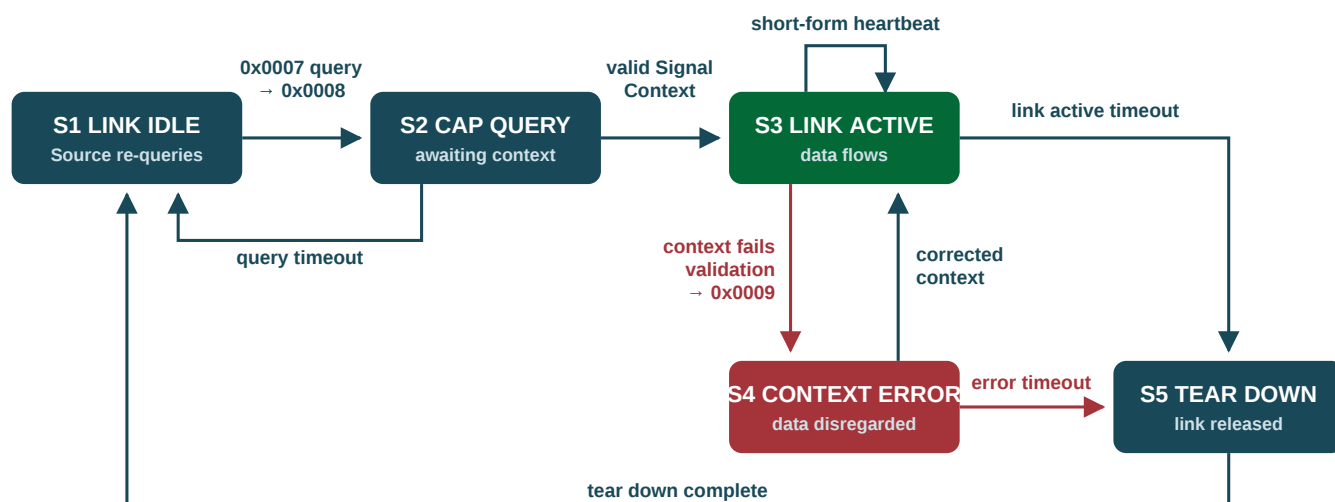
INTERFACES

AXI4-Stream (data), AXI4-Lite (control and status)

PERFORMANCE

32-bit data path, 1 GbE reference design

LINK ESTABLISHMENT, IN HARDWARE



The negotiation runs entirely in programmable logic. The Sink answers every capability query, validates each Signal Context, and reports faults in band — no host involvement on the critical path.

PURCHASE INCLUDES

- AMD: Zynq reference design
 - Picozed 7030 FMC2 with 1 GbE
- Software and Tooling
 - Host C++ demonstration applications
 - DIFI 1.3 Wireshark dissector
 - DIFI Consortium certification harness
 - VHDL testbench
- Embedded Support
 - Yocto/PetaLinux utilities

DELIVERY OPTIONS

- Encrypted code: Protected source
- Source code: Fully modifiable

LICENSING

Site-wide: The core may be used on all projects within the organization.

GET STARTED

- Request Evaluation License
- Contact Sales vita49@geontech.com for Pricing