STANDARDS-COMPLIANT FPGA COMMUNICATIONS

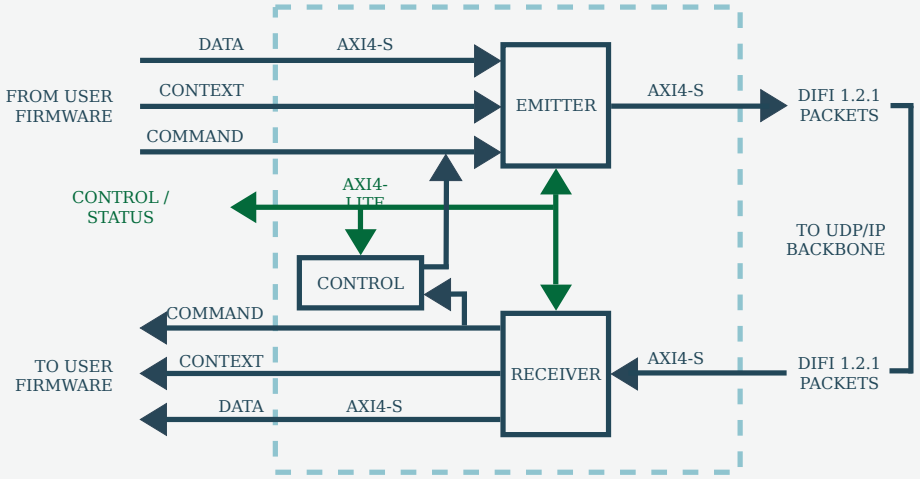
DIFI 1.2.1

An FPGA IP core for the DIFI 1.2.1 digital IF standard — every Information Class parsed and encapsulated in fabric

KEY BENEFITS

- All five DIFI 1.2.1 Information Classes
- Data, Context and Flow Control packets
- Transport agnostic (UDP/IP, PCIe, Aurora)
- Rapid AXI-based integration
- Reference designs for 1/10 GbE
- RX-only and TX-only builds to save fabric

DIFI 1.2.1 IP CORE



CORE FEATURES

INFORMATION CLASSES

Basic Data Plane, Version Flow, Data Plane + Flow Control, Data Plane + Flow Control Real Time TSF, and Basic Data Plane Sample Count TSF.

PACKET CLASSES

Seven classes across Signal Data, Signal Context, Version Context and Timing Flow Control.

INTERFACES

AXI4-Stream (data), AXI4-Lite (control and status)

PERFORMANCE

1/10 GbE (32-bit) and up to 100 GbE (512-bit)

RESOURCE OPTIMIZATION

RX-only and TX-only configurations drop the unused half of the core.

PORTABILITY

FPGA vendor independent; only the FIFO primitives are vendor-specific and are swappable.

CONTACT

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WHAT THE CORE HANDLES

INFORMATION CLASS	PACKET CLASSES CARRIED
0x0000 Basic Data Plane	Standard Flow Signal Data, Standard Flow Signal Context
0x0001 Version Flow	Version Flow Signal Context
0x0002 Data Plane + Flow Control	Sample Count Signal Data, Sample Count Signal Context, Sample Count Timing Flow Control
0x0003 Data Plane + FC, Real Time TSF	Standard Flow Signal Data, Standard Flow Signal Context, Real Time TSF Timing Flow Control
0x0004 Basic Data Plane, Sample Count TSF	Sample Count Signal Data, Sample Count Signal Context

Every Information Class in DIFI 1.2.1, with the packet classes each one carries. Signal Data in green, Signal Context in blue, Timing Flow Control in grey — all parsed and encapsulated in programmable logic.

PURCHASE INCLUDES

- AMD: Zynq / UltraScale+ reference designs
  - Picozed 7030 FMC2 with 1 GbE
  - ZCU102 with 10 GbE
  - ZCU111 with 10 GbE
  - ZCU208 with 10 GbE
  - ZCU216 with 10 GbE
- Software and Tooling
  - Host C++ packet processing software
  - Wireshark plugin
  - VHDL testbench
- Embedded Support
  - Yocto/PetaLinux utilities

DELIVERY OPTIONS

- Encrypted code: Protected source
- Source code: Fully modifiable

LICENSING

Site-wide: The core may be used on all projects within the organization.

GET STARTED

- Request Evaluation License
- Contact Sales vita49@geontech.com for Pricing

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